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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/686,958	10/12/2000	Shinsuke Nakajyo	001344	5708

7590 09/03/2003

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EXAMINER
LUHRS, MICHAEL K

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/686,958	NAKAJYO ET AL.	
	Examiner	Art Unit	
	Michael K. Luhrs	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/11/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan et. al. (USPN 4,967,146) in view of Glenn (USPN 6,228,676) and Corbett (USPN 5,383,361). Regarding claim 1, Morgan et. al. teach of *conducting electrical test to each chip* by a testing process, that includes markings row and column of each die (line 55 column 4), with *positional information* as shown in Fig. 2 and as described explicitly in column 2, lines 57-64, is a *first marking*. Since Morgan et. al. indicate that prior art practice has been to assemble the chips into a finished product before testing, (lines 60-62 column 4), their solution is to conduct the testing of the chips as they reside on the wafer (as indicated in Morgan et. al.'s claims 4 and 5) and marking as a function of the tested chips, (see line 23, column 7 of claim 5) is the *second marking of the result of the electrical test*. Morgan et. al. teach of the subsequent *dicing* in lines 1-3 column 5 wherein the wafer is broken into the individual device chips—see the last action of Morgan et. al.'s claim 5. Morgan et. al. are silent to the first and second marking at the *rear* surface of the wafer. Morgan et. al. provide a photoresist on the wafer (line 15 column 4) to define the groove lines for dicing but are silent regarding the photoresist as a sealant, are thus silent regarding *sealing with a resin material*. Glenn et. al. teach of the sealing resin, encapsulant, 42, line 40 column 7. Glenn et. al. disclose *sealing the front surface of a wafer having the front and rear surfaces and having a plurality of semiconductor chips on the front surface with resin material*, by coating the front surface with encapsulant insulation, 42, line 37 column 6. Since Morgan et. al. and Glenn et. al. are all from the same

field of endeavor, the purpose disclosed by Glenn et. al. would have been recognized in the pertinent art of Morgan et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill to add the sealing process of coating with encapsulant as taught by Glenn et. al. to the process of Morgan et. al. to generate an insulative barrier. Corbett teach of marking the chip using a laser marking and teach that marking can be provided on either side of a chip line 10 column 5 or entire wafer line 47, column 4, since both sides are exposed (line 11, column 5). Since Morgan et. al., Glenn et. al. and Corbett are all from the same field of endeavor, the purpose disclosed by Corbett would have been recognized in the pertinent art of Morgan et. al. and Glenn et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art that the chip could be marked on either side as taught by Corbett and that the **test result** taught by Glenn et. al. could thus be marked on the *rear* side.

Regarding claim 2, Morgan et. al. teach *conducting electrical test to each chip* by way of a testing process, discussed above for claim 1, and teach *marking in the region of each chip at the surface of the wafer, the position information*, by including markings row and column of each die (line 55 column 4), with *positional information* as shown in Fig. 2 and as described explicitly in column 2, lines 57-64 (discussed above for claim 1) and Morgan et. al. teach of the subsequent *dicing* in lines 1-3 column 5 wherein the wafer is broken into the individual device chips—see the last action of Morgan et. al.'s claim 5 (also discussed above for claim 1), but fails to seal and provide marking on *rear* surface. Glenn et. al. teach of the sealing resin. Corbett teach of marking either side. It would have been obvious at the time the invention was made to a person having ordinary skill in the art that the chip could be marked on either side as taught by Corbett and that the **positional marking** and test results (line 23 column 7) taught by Morgan et. al. could thus be marked on either side as taught by Corbett, which includes the *rear* side.

2. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan et. al., Glenn, and Corbett as applied to claims 1 or 2 above, and further in view of Ohgiyama (USPN 6,309,909).

Regarding claim 3, Morgan, et. al. teach photoresist (line 15, column 4) (a photoresist includes a resin, typically phenolic resin) on either side of wafer as they discuss in lines 17-24, column 4, yet fail to teach *sealing* with resin on circuit surface and opposite surface. Glenn et. al., teach the resin encapsulant on the circuit side, see for example Fig 1 showing layer 42 is on the circuit side of substrate 12, but fail to teach the resin on the opposite surface. Corbett teach of the laser markings using resinous material, not sealing. Ohgiyama teaches that a resist layer 20 can act as a sealant by preventing moisture from entering the interface between the sealing resin and the pads at the opposite surface, (see lines 29-33, column 10). Since Ohgiyama and Morgan et. al., Glenn et. al., and Corbett are all from the same field of endeavor, the purpose disclosed by Ohgiyama would have been recognized in the pertinent art of Morgan et. al., Glenn et. al., and Corbett. It would have been obvious at the time the invention was made to a person having ordinary skill in the art that the photoresist resin provided by Morgan et. al. could also act as a sealing resin as taught by Ohgiyama. The *result of electrical test are marked in the region of each chip on the surface*, has been discussed for claim 1 above, and is not reiterated.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et. al. in view of Corbett.

Glenn et. al. teach of sealing the front surface of a wafer, with encapsulant layer 42. Glenn et. al. dice the wafer, as in cutting, in lines 32-34 column 7. Glenn et. al. teach of attaching a resin sheet, as in mounting tape (line 45 column 7), but fails to teach the rear surface and marking to indicate position on the sheet. Corbett discloses a ribbon of resinous material having ink bearing material applied to the wafer for marking purposes, (line 49 and 63, column 2). Positional information is taught Corbett in line 19, column 1 (see, "lot number or die location"). Since Corbett and Glenn et. al. are both from the same field of endeavor, the purpose disclosed by Corbett would have been recognized in the pertinent art of Glenn et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to add the resin as taught by Corbett to aid in facilitating the marking of the chips (line 43, column

7, in Corbett) with positional information as discussed in lines 18-19, column 1. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include positional information as taught by Corbett in the process Glenn et. al. who teaches of wafer level semiconductor manufacturing in general.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et. al. and Corbett as applied to claim 4 above, and further in view of Morgan et. al..

Regarding claim 5, Glenn et. al. teach testing in line 46 column 7. Glenn et. al. is silent on the marking of the test result. Corbett teach marking operation on either side but are silent regarding testing results. Morgan et. al. teaches marking with test results, line 23, column 7 (i.e. Morgan et. al.'s claim 5). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include marking of test results as taught by Morgan et. al. in the process taught by Glenn et. al. who teaches of wafer level semiconductor manufacturing in general and further that such marking of test results could be provided on the rear side as indicated by Corbett who teaches that laser marking in general in not restricted to a particular side (lines 9-10 column 5).

Response to Arguments

5. The following response to applicant's "Request for Reconsideration" dtd 6/11/03, is provided:

a. Applicant asserts (line 14, p. 2 of applicant's "Request for Reconsideration") "chips 30 mounted on the substrate are already diced when the chips are sealed with resin" referring to the Glenn et. al. patent. Examiner respond... applicant's referral to the dicing of the chips is misguided, rather the Glenn et. al. 'substrate' 13 (line 60, col. 6 and line 24, col. 5) does not have to be diced when sealed (see the dam 59 lines 58-60 col. 6 for the sealing encapsulant area, the reference to Fig. 3B showing substrate 13, and then Fig. 3A showing 13, having chips and chip area 12), and substrate is consistent with the applicant's wafer.

b. Applicant asserts (line 4, p. 3 of applicant's "Request for Reconsideration") "Morgan et. al. teaches marking wafer while Corbett teaches marking to chip", is inaccurate, since Corbett et. al. mentions entire wafer in line 47, col. 4.

c. Applicant asserts (line 8, p. 3 of applicant's "Request for Reconsideration") "Morgan et. al., Glenn et. al. nor Corbett patents disclose marking a rear surface of a wafer", is inaccurate, since Corbett et. al. mentions either side in line 10, col. 5.

d. Regarding applicant's last paragraph p. 3 of "Request for Reconsideration", the examiner would add that Corbett was presented for 'rear side and positional' info, Glenn et. al. may have lacked, whereas Glenn et. al. has the resin as blue mount tape line 28 col. 7, is indicative of a resin sheet.

e. Applicant's argument to the addition of Ohgiyama to the Morgan et. al., Glenn et. al. and Corbett patents for remaining claims does not include any persuasive information at all, so the rejection is maintained. Ohgiyama is explicit in lines 24-37 col. 8 and lines 29-33 col. 10, regarding marking and resin.

f. Applicant refers to "dependent claim 4" line 3, p.1, second full paragraph of applicant's "Request for Reconsideration", however claim 4 is an independent claim is obvious error by the

applicant in describing their own claim. However should the applicant not be aware that independent claim 4 had a rejection (Glenn et. al. in view of Corbett) it can be referred to above, (item 3). Thus and furthermore, there is lack of persuasive argument on the applicant's part to address the rejection to independent claim 4, rather applicant refers to "ink ribbon" (p. 3,line 12, of applicant's "Request for Reconsideration") in Corbett which is misguided, since Glenn et. al. clearly already provides a resinous sheet, as the blue wafer mounting tape in line 28, col. 7. In reference to any argument that the applicant may have included in the last paragraph of p. 3 of applicant's "Request for Reconsideration" for claim 5, the examiner would respond that the argument is misguided since the reasoning in claim 4 was premature to Corbett since Glenn et. al. provides resinous sheet as mentioned above.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael K. Luhrs whose telephone number is 703-305-2864. The examiner can normally be reached on M-F; 8:00 a.m. - 5:00 p.m. (other Fridays off)..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 703-308-2816. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MKL

Michael K. Luhrs

9/1/03

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER